IN THE CLAIMS:

Please amend claims 1, 3, 5, 6, and 8, and add new claims 18-28 as follows:

1. (Currently Amended) An injection mold for encapsulating an integrated circuit chip in an encapsulation material so as to form a semiconductor package containing the chip, said injection mold comprising:

at least one injection cavity ~~for housing~~ defined by a wall, the injection cavity being able to house the chip and receive the encapsulation material so as to encapsulate the chip in a block of the encapsulation material; and

an insert having a front part that forms ~~part~~ a first portion of the wall of the injection cavity and a transverse surface that lies parallel to one face of the chip,

wherein the transverse surface of the insert has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert.

2. (Original) The injection mold according to claim 1, wherein the insert protrudes into the interior of the injection cavity so as to form a hollow in the package in the region corresponding to the transverse surface of the insert.

3. (Currently Amended) The injection mold according to claim 2, further comprising a blind annular space around at least a part of the insert, the blind annular space emerging ~~that emerges~~ in the injection cavity.

4. (Original) The injection mold according to claim 1, wherein the front part of the insert has a protruding transverse surface surrounded by an annular shoulder that is set back with respect to the protruding transverse surface.

5. (Currently Amended) The injection mold according to claim 4, further comprising a blind annular space around at least a part of the insert, the blind annular space emerging ~~that emerges~~ in the injection cavity.

6. (Currently Amended) The injection mold according to claim 1, further comprising a blind annular space around at least a part of the insert, the blind annular space emerging ~~that emerges~~ in the injection cavity.

7. (Original) The injection mold according to claim 6, wherein the annular space is enlarged in a part remote from the injection cavity.

8. (Currently Amended) The injection mold according to claim 1, further comprising:

first and second parts having a parting line and between ~~which~~ them defining the injection cavity ~~is defined~~,

wherein the first part ~~carries~~ has a passage in which the insert is fixed in such a way that the transverse surface of the ~~inverse~~ insert lies parallel to the parting line of the first and second parts, and

the second part is provided with at least one movable demolding member opposite the insert and means for keeping the demolding member bearing on the package when the second part of the mold is separated from the first part of the mold during demolding.

9. (Original) The injection mold according to claim 8, wherein the first part of the mold includes pushers for demolding the package.

10-17. (Canceled)

18. (New) The injection mold according to claim 1, further comprising a first part that forms a second portion of the wall of the injection cavity, the first part having a passage in which the insert is fixed such that the front part of the insert forms the first portion of the wall of the injection cavity.

19. (New) The injection mold according to claim 18, further comprising a second part that forms a third portion of the wall of the injection cavity, the first and second parts having a parting line and between them defining the injection cavity.

20. (New) An injection mold for encapsulating an integrated circuit chip in an encapsulation material so as to form a semiconductor package containing the chip, said injection mold comprising:

a first part and a second part having a parting line, the first part having a passage;

at least one injection cavity defined between the first and second parts, the injection cavity being able to house the chip during encapsulation; and

an insert fixed in the passage of the first part such that a front part of the insert forms a portion of the wall of the injection cavity, the insert having a transverse surface that lies parallel to one face of the chip,

wherein the transverse surface of the insert has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert.

21. (New) A semiconductor package formed in the injection mold according to claim 1, said semiconductor package comprising:

an encapsulation block having a transverse face; and

at least one integrated circuit chip contained in the encapsulation block, one face of the chip including an optical sensor and lying parallel to the transverse face of the encapsulation block,

wherein the material of the encapsulation block that encapsulates the chip is transparent, and

the transverse face of the encapsulation block includes a region located opposite the optical sensor that has a roughness that is less than the roughness of at least the rest of the transverse face of the encapsulation block.

22. (New) The semiconductor package according to claim 21, wherein the region at least covers the optical sensor of the chip.

23. (New) The semiconductor package according to claim 21, wherein the roughness of the region is less than 0.10.

24. (New) The semiconductor package according to claim 21, wherein the roughness of the region is less than 0.07.

25. (New) An information processing system including at least one optical semiconductor package formed in the injection mold according to claim 1, said optical semiconductor package comprising:

an encapsulation block having a transverse face; and

at least one integrated circuit chip contained in the encapsulation block, one face of the chip including an optical sensor and lying parallel to the transverse face of the encapsulation block,

wherein the material of the encapsulation block that encapsulates the chip is transparent, and

the transverse face of the encapsulation block includes a region located opposite the optical sensor that has a roughness that is less than the roughness of at least the rest of the transverse face of the encapsulation block.

26. (New) The information processing system according to claim 25, wherein the region of the transverse face of the encapsulation block of the optical semiconductor package at least covers the optical sensor of the chip.

27. (New) The information processing system according to claim 25, wherein the roughness of the region of the transverse face of the encapsulation block of the optical semiconductor package is less than 0.10.

28. (New) The information processing system according to claim 25, wherein the roughness of the region of the transverse face of the encapsulation block of the optical semiconductor package is less than 0.07.